What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory device comprising:

a memory array;

a control circuit coupled to the memory array;

at least one of configuration line coupled to said control circuit;

wherein said control circuit operates the memory device at a selected device read latency based upon a state of a signal asserted on said at least one configuration line.

2. The memory device of claim 1, wherein said set of device read latencies includes the memory device's minimum device read latency.

3. The memory device of claim 1, wherein said control circuit interprets the state of signals asserted on said first plurality of configuration lines as a number of clock cycles and operates the memory device at a device read latency equal to the minimum device read latency plus the number of clock cycles.

4. The memory device of claim 1, wherein the control circuit, responsive to a command issued by an external memory controller, outputs to said memory controller a calibration pattern as read data.

5. The memory device of claim 4, wherein said calibration pattern includes at least two successive bits which have a different logic state.

6. The memory device of claim 5, wherein said calibration pattern has its first bit set to a binary 0 and all subsequent bits set to a binary 1.

7. The memory device of claim 5, wherein said calibration pattern has its first bit set to a binary 1 and all subsequent bits set to a binary 0.

8. The memory device of claim 1, wherein said at least one configuration line includes a plurality of configuration lines.

9. The memory device of claim 1, wherein the set of device read latencies includes N device latencies ranging from the device minimum read latency to a number of clock cycles equal to the device minimum read latency plus N-1 clock cycles.

10. The memory device of claim 9, wherein N equals 8.

11. The memory device of claim 1, further comprising:

an additional configuration line, wherein said additional configuration line has a signal state which enables or disable a read clock delay lock loop of said memory device.

12. A memory module comprising:

a plurality of memory devices; and

a register for providing configuration information to said plurality of memory devices;

wherein each of said memory device further comprises,

a memory array;

a control circuit coupled to the memory array;

at least one of configuration line coupled to said register and said control circuit;

wherein said control circuit operates the memory device at a selected device read latency based upon a state of a signal asserted on said at least one configuration line.

13. The memory module of claim 12, wherein said set of device read latencies includes the memory device's minimum device read latency.

14. The memory module of claim 12, wherein said control circuit interprets the state of signals asserted on said at least one configuration line as a number of clock cycles and operates the memory device at a device read latency equal to the minimum device read latency plus the number of clock cycles.

15. The memory module of claim 12, wherein the control circuit, responsive to a command issued by an external memory controller, outputs to said memory controller a calibration pattern as read data.

16. The memory module of claim 15, wherein said calibration pattern includes at least two successive bits which have a different logic state.

17. The memory module of claim 16, wherein said calibration pattern has its first bit set to a binary 0 and all subsequent bits set to a binary 1.

18. The memory module of claim 16, wherein said calibration pattern has its first bit set to a binary 1 and all subsequent bits set to a binary 0.

19. The memory module of claim 12, wherein said at least one configuration line includes a plurality of configuration lines.

20. The memory module of claim 12, wherein the set of device read latencies includes N device latencies ranging from the device minimum read latency to a number of clock cycles equal to the device minimum read latency plus N-1 clock cycles.

21. The memory module of claim 20, wherein N equals 8.

22. The memory module of claim 12, further comprising:

an additional configuration line, wherein said additional configuration line has a signal state which enables or disable a read clock delay lock loop of said memory device.

23. A method of operating a memory device, the memory device having at least one configuration line, comprising:

operating the memory device at a selected device read latency based upon a state of a signal asserted on said at least one configuration line.

24. The method of claim 23, wherein said set of device read latencies includes the memory device's minimum device read latency.

25. The method of claim 23, wherein said control circuit interprets the state of the signal asserted on said at least one configuration line as a number of clock cycles and operates the memory device at a device read latency equal to the minimum device read latency plus the number of clock cycles.

26. The method of claim 23, further comprising the step of:

responsive to a command from a memory controller, outputting a calibration pattern.

27. The method of claim 26, wherein said calibration pattern includes at least two successive bits which have a different logical state.

28. The method of claim 27, wherein said calibration pattern has its first bit set to a binary 0 and all subsequent bits set to a binary 1.

29. The method of claim 27, wherein said calibration pattern has its first bit set to a binary 1 and all subsequent bits set to a binary 0.

30. The method of claim 23, wherein said at least one configuration line includes a plurality of configuration lines.

31. A computer system comprising:

a processor;

a memory controller coupled to the processor;

at least one memory module coupled to the memory controller, each of said memory modules comprising a plurality of memory devices;

wherein each of said memory devices further comprises,

a memory array;

a control circuit coupled to the memory array;

at least one configuration line coupled to said control circuit;

wherein said control circuit operates the memory device at a selected device read latency based upon a state of a signal asserted on said at least one configuration line.

32. The computer system of claim 31, wherein said set of device read latencies includes the memory device's minimum device read latency.

33. The computer system of claim 31, wherein said control circuit interprets the state of a signal asserted on said at least one configuration line as a number of clock cycles and operates the memory device at a device read latency equal to the minimum device read latency plus the number of clock cycles.

34. The computer system of claim 31, wherein the control circuit, responsive to a command issued by an external memory controller, outputs a calibration pattern.

35. The computer system of claim 34, wherein said calibration pattern includes at least two successive bits which have a different logical state.

36. The computer system of claim 35, wherein said calibration pattern has its first bit set to a binary 0 and all subsequent bits set to a binary 1.

37. The computer system of claim 35, wherein said calibration pattern has its first bit set to a binary 1 and all subsequent bits set to a binary 0.

38. The computer system of claim 31, wherein said at least one configuration line includes a plurality of configuration lines.

39. The computer system of claim 31, wherein the set of device read latencies includes N device latencies ranging from the device minimum read latency to a number of clock cycles equal to the device minimum read latency plus N-1 clock cycles.

40. The computer system of claim 39, wherein N equals 8.

41. A method of operating a memory system, the memory system having at a plurality of memory devices and a memory controller, comprising the steps of:

responsive to a command from the memory controller, setting each of the plurality of memory devices to operate at its minimum device read latency;

measuring the system read latency for each of the plurality of memory devices at said memory controller;

determining a maximum system read latency at said memory controller, said maximum system read latency being equal to the maximum of the plurality of system read latencies;

calculating a plurality of offsets at said memory controller, each of said plurality of offsets being associated with a corresponding one of the plurality of memory devices and being equal to the difference between the maximum system read latency and the system read latency of the corresponding one of the plurality of memory devices; and

setting each of the plurality of memory devices to operate at an increased device read latency by the memory controller, wherein the amount of increased device read latency is equal to the offset associated with that one of the plurality of memory devices.

42. The method of claim 41, wherein the step of measuring further comprises:

sending a calibration pattern from each memory device in response to a command from said memory controller.

43. The method of claim 42, wherein said calibration pattern includes at least two successive bits which have a different logical state.

44. The method of claim 43, wherein said calibration pattern has its first bit set to a binary 0 and all subsequent bits set to a binary 1.

45. The method of claim 44, wherein said calibration pattern has its first bit set to a binary 1 and all subsequent bits set to a binary 0.